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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,006	09/04/2003	Brian Peng	JCLA11225	8164

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IRVINE, CA 92618

EXAMINER	
TERESINSKI, JOHN	
ART UNIT	**PAPER NUMBER**
2858	

DATE MAILED: 05/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/656,006	PENG ET AL.
	Examiner	Art Unit
	John Teresinski	2858

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8* is/are rejected.

7)☒ Claim(s) *9-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 9-15 are objected to because of the following informalities: Claim 8 recites a "DVD ROM chipset testing board" while claims 9-15 recite the "DVD ROM testing board as recited in claim 8" providing unclear claim recitations. Appropriate correction is required.

Claim Rejections - 35 USC § 103

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2003/0101391 to Man et al. in view of U.S. Patent No. 5,663,966 to Day et al..

Regarding claim 8, Man et al. disclose a system for testing multiple devices on a single system and method having a testing base (Fig. 4, element 420), having at least one chip socket (434) for plugging the DVD ROM chip-set (paragraph 13), and a connector (425) for coupling to a testing device of the DVD ROM chipset, wherein the testing device provides a digital input signal/command signals (paragraph 13). Man et al. does not disclose phase -shift RF-signal generating circuits according to the input test signals. Day et al. disclose a system and method for scan based testing including a testing device providing a digital input signal with varied frequency (column 8 lines 8-14), a phase-shift RF-signal generating circuit (column 8 lines 13-45), according to the digital data input signal, for generating a first phase-shift RF-signal, a second phase-shift RF signal, a third phase-shift RF signal, and a fourth phase-shift RF signal for testing a chipset/chip wherein the first phase-shift RF signal and the second phase-shift RF signal are in phase, and are differed by a phase shift from the third phase-shift RF signal and fourth

phase-shift RF signal (column 8 lines 48-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the phase-shift RF signal generating circuits as taught by Day et al. into Man et al. for the purpose of allow concurrent testing of multiple section of one or more chips under scan test and to reduce simultaneous switching.

Allowable Subject Matter

Claims 9-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

Regarding claim 9:

The primary reason for the allowance of claim 9 is the inclusion of first and second potential dividers and first, second third and fourth high pass filters. It is these features found in the claim, as they are claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes this claim allowable over the prior art.

Claims 10-15 would be allowed due to dependency on claim 9.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following is cited to further show the state of the art with respect to methods and devices for testing chipsets:

U.S. Patent No. 6,880,116 to Man et al. disclose a system for testing multiple devices on a single system.

U.S. Patent Application Publication No. 2003/0057940 to Tanimura discloses a testing board apparatus including a timing generator for generating multiple input signals.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Teresinski whose telephone number is (571) 272-2235. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lefkowitz can be reached on (571) 272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JT

JT
May 5, 2005

ANJAN DEB
PRIMARY EXAMINER